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WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a semiconductor wiring substrate including a plurality of wires;

a chip IP including a circuit having semiconductor device elements arranged therein, the chip IP being attached to and mounted on the semiconductor wiring substrate so that the circuit is electrically connected to the plurality of wires of the semiconductor wiring substrate; and

at least one test pad connected to at least one of the wires of the semiconductor wiring substrate for testing an electrical connection between the circuit of the chip IP and the wires.

2. The semiconductor device of claim 1, wherein the test pad is an external terminal pad of the semiconductor device.

3. The semiconductor device of claim 1, wherein the test pad is a portion of the at least one of the wires that is exposed on a surface of the semiconductor wiring substrate.

4. The semiconductor device of claim 1, wherein:

the circuit of the chip IP includes a power supply line for supplying a power supply voltage and a node forming a protection diode between the power supply line and the node; and

the test pad includes a first test pad connected to a wire that is connected to the power supply line and a second

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test pad connected to a wire that is connected to the node in the circuit.

5. The semiconductor device of claim 1, wherein:

the circuit of the chip IP includes a ground line for supplying a ground voltage and a node forming a protection diode between the ground line and the node; and

the test pad includes a first test pad connected to a wire that is connected to the ground line and a second test pad connected to a wire that is connected to the node in the circuit.

6. The semiconductor device of claim 1, wherein:

the circuit of the chip IP includes a ground line for supplying a ground voltage, a power supply line for supplying a power supply voltage, and a selector for receiving, and selectively outputting one of, a signal of the ground line or the power supply line and an output signal of an output section of the circuit; and

the test pad includes a first test pad connected to a wire for supplying a switching control signal for the selector and a second test pad connected to an output section of the selector.

7. The semiconductor device of claim 1, wherein a switching element for turning ON/OFF transmission of a signal from the test pad is provided at a position that is along each of the plurality of wires of the semiconductor wiring substrate connected to the test pad and opposite to the chip

IP with respect to the test pad.

8. The semiconductor device of claim 1, further comprising:

a test circuit provided in the chip IP for testing an electrical connection between the circuit of the chip IP and the wires; and

a setting circuit for setting at least the test circuit in a test mode,

wherein the test pad includes a first test pad for supplying a test mode signal to the test circuit and the setting circuit and a second test pad for receiving an output of the test circuit.

9. The semiconductor device of claim 8, wherein the test circuit has a pull-down type circuit structure or a pull-up type circuit structure.

10. The semiconductor device of claim 8, wherein the setting circuit is provided in the chip IP.

11. The semiconductor device of claim 8, wherein the setting circuit is provided in a chip different from the chip IP.

12. The semiconductor device of claim 8, wherein:

the circuit of the chip IP includes a power supply line for supplying a power supply voltage and a ground line for supplying a ground voltage; and

the semiconductor device further comprises:

a third pad connected to a wire that is connected to

the power supply line; and

a fourth pad connected to a wire that is connected to the ground line.

13. A method for testing a semiconductor device, the semiconductor device including: a semiconductor wiring substrate including a plurality of wires; and a chip IP including an internal circuit, the internal circuit including a power supply line for supplying a power supply voltage and a node forming a protection diode between the power supply line and the node, the chip IP being attached to and mounted on the semiconductor wiring substrate so that the internal circuit is electrically connected to the plurality of wires of the semiconductor wiring substrate,

the method comprising, after forming a first test pad connected to one of the plurality of wires that is connected to the power supply line and a second test pad connected to another one of the plurality of wires that is connected to the node in the circuit, the steps of:

(a) supplying a voltage lower than a voltage of the power supply line via the first test pad to the power supply line; and

(b) detecting a voltage or a current at the node of the circuit via the second test pad, thereby testing an electrical connection between the circuit of the chip IP and the plurality of wires.

14. A method for testing a semiconductor device, the

semiconductor device including: a semiconductor wiring substrate including a plurality of wires; and a chip IP including an internal circuit, the internal circuit including a ground line for supplying a ground voltage and a node forming a protection diode between the ground line and the node, the chip IP being attached to and mounted on the semiconductor wiring substrate so that the internal circuit is electrically connected to the plurality of wires of the semiconductor wiring substrate,

the method comprising, after forming a first test pad connected to one of the plurality of wires that is connected to the ground line and a second test pad connected to another one of the plurality of wires that is connected to the node in the circuit, the steps of:

(a) supplying a voltage higher than a voltage of the ground line via the first test pad to the ground line; and

(b) detecting a voltage or a current at the node of the circuit via the second test pad, thereby testing an electrical connection between the circuit of the chip IP and the plurality of wires.

15. A method for testing a semiconductor device, the semiconductor device including: a semiconductor wiring substrate including a plurality of wires; and a chip IP including an internal circuit, the internal circuit including a power supply line for supplying a power supply voltage and a node forming a protection diode between the power supply

line and the node, the chip IP being attached to and mounted on the semiconductor wiring substrate so that the internal circuit is electrically connected to the plurality of wires of the semiconductor wiring substrate,

the method comprising, after forming a test circuit in the chip IP for testing an electrical connection between the circuit of the chip IP and the wires and a setting circuit for setting the circuit in the chip IP and the test circuit in a test mode,

and after forming a first test pad connected to one of the plurality of wires that is connected to the setting circuit and a second test pad connected to another one of the plurality of wires that is connected to the test circuit, the steps of:

(a) inputting a test mode setting signal via the first test pad to the setting circuit and the test circuit; and

(b) detecting an output of the test circuit via the second test pad, thereby testing the electrical connection between the circuit of the chip IP and the plurality of wires.

16. The method for testing a semiconductor device of claim 15, wherein:

the test circuit is formed to have a pull-down type circuit structure;

in the step (a), the test mode setting signal is input so that an H-level signal is output from the setting

circuit; and

in the step (b), the electrical connection between the chip IP and the plurality of wires is determined to be good when the output from the test circuit is at an H level.

17. The method for testing a semiconductor device of claim 15, wherein:

the test circuit is formed to have a pull-up type circuit structure;

in the step (a), the test mode setting signal is input so that an L-level signal is output from the setting circuit; and

in the step (b), the electrical connection between the chip IP and the plurality of wires is determined to be good when the output from the test circuit is at an L level.

18. The method for testing a semiconductor device of claim 15, wherein:

a plurality of the chip IPs are provided;

the circuit of each chip IP includes a power supply line for supplying a power supply voltage and a ground line for supplying a ground voltage;

the semiconductor device further comprises:

a third pad connected to a wire that is connected to the power supply line;

a fourth pad connected to a wire that is connected to the ground line;

a switching device for turning ON/OFF an electric

conduction of a wire between the chip IPs; and

a selector for switching outputs from the respective chip IPs from one to another,

wherein the switching device and the selector are controlled by the setting circuit so that the steps (a) and (b) are performed successively for each of the chip IPs.

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